UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,298	10/20/2003	Tommy Hsiao	184-P065D1C1	4293

7590 01/11/2006

Michael P. Adams
Winstead Sechrest & Minick P.C.
P.O.BOX 50784
Dallas, TX 75201

EXAMINER	
RICHARDS, N DREW	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 01/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/689,298
Filing Date: October 20, 2003
Appellant(s): HSIAO ET AL.

Michael P. Adams
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 10/17/05 appealing from the Office action mailed 6/14/05.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

GROUNDS OF REJECTION NOT ON REVIEW

The following grounds of rejection have not been withdrawn by the examiner, but they are not under review on appeal because they have not been presented for review in the appellant's brief. Claims 1, 3-9 and 17-26 are rejected under the judicially created doctrine of obviousness-type double patenting.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-5, 7, 8, 17 and 19-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al. (USPAT 5482881, Chen).

With regard to claim 1, Chen discloses in figures 3 and 6 a method for providing a semiconductor memory device including a substrate (116) and at least one field isolation region (300). Chen discloses in figures 3 and 6 providing (450) a plurality of gate stacks (700) above the substrate, each of the plurality of gate stacks including a first edge and a second edge, each of the plurality of gate stacks crossing the at least one field isolation region (300). Chen discloses in figures 3, 6 – 6c, and 6f providing a source implant (458/670, DDI/MDDI, 112) adjacent to the first edge of each of the plurality of gate stacks. Chen discloses in figures 3, 6, and 6d driving (462) the source implant under the first edge of each of the plurality of gate stacks. Chen discloses in figures 3, 6, 6e, and 6f providing a drain implant (672, MDD2, 114,) after, the drain implant being provided in the substrate adjacent to the second edge of each of the plurality of gate stacks.

With regard to claim 3, Chen discloses in figures 3 and 6 – 6f wherein the source implant providing step includes the step of providing a first source implant (DDI) and a second source implant (MDD1) adjacent to the first edge of each of the plurality of gate stacks. Chen discloses in figures 3 and 6 – 6f wherein the driving step includes the step of driving the first source implant and the second source implant under the first edge of each of the plurality of gate stacks.

With regard to claim 4, Chen discloses in figures 3, 6, 6b – 6d, and 6f further comprising the step of providing a first spacer and a second spacer (both formed of

insulating layer 720) for each of the plurality of gate stacks, the first spacer being disposed along the first edge of each of the plurality of gate stacks, the second spacer being disposed along the second edge of each of the plurality of gate stacks.

With regard to claim 5, Chen discloses in figures 3 and 6 – 6a further comprising the step of providing a self-aligned source etch (454).

With regard to claim 7, Chen teaches wherein the drain implant (MDD2) is As (arsenic). Though not explicitly stated, it is implicitly understood that the drain implant is arsenic as Chen teach on the first paragraph of column 7 and on column 8 line 18 through column 9 line 9, that the same dopant is used for the MDD implants and that arsenic is used as the MDD implant dopant.

With regard to claim 8, Chen discloses in figures 3 and 6 – 6f and column 8, lines 19 – 52 wherein the second source implant is As.

With regard to claim 17, Chen discloses in figures 3, 6, and 6d wherein the step of driving the source implant under the first edge of each of the plurality of gate stacks comprises a thermal treatment (462).

With regard to claim 19, Chen discloses in figures 3 and 6 – 6f forming a gate stack. Chen discloses in figures 3 and 6 – 6f performing a source implant adjacent to a first edge of the stacked gate. Chen discloses in figures 3 and 6 – 6f heat treating the semiconductor memory so that the source implant diffuses under the first edge of the stacked gate. Chen discloses in figures 3 and 6 – 6f, after the source implant diffuses under the first edge of the stacked gate, performing a drain implant adjacent to a second edge of the stacked gate. Chen discloses in figures 3 and 6 – 6f the source

implant extends further under the first edge of the stacked gate than the drain implant extends under the second edge of the stacked gate.

With regard to claim 20, Chen discloses in figures 3 and 6 – 6f wherein performing the source implant comprises performing a double diffused implant (DDI).

With regard to claim 21, Chen discloses in figures 3 and 6 – 6f wherein performing the source implant comprises performing a double diffused implant (DDI), and performing a moderately doped drain implant (MDDI).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (USPAT 5482881, Chen) as applied to claims 1, 3-5, 7, 8, 17 and 19-21 above, and further in view of Gardner et al. (USPAT 5953613, Gardner).

With regard to claim 9, Chen discloses in figure 6 oxidizing after the drain implant has been provided. It is not clear if Chen further teaches comprising the step of providing a rapid thermal anneal after the drain implant has been provided. Gardner further teaches in column 7, lines 49 – 52 comprising a step of providing a rapid thermal anneal after a drain implant has been provided. It would have been further obvious to one of ordinary skill in the art at the time of the present invention to use the rapid

thermal annealing step of Gardner in the method of Chen and Gardner in order to activate the drain dopants and remove crystalline damage as taught by Gardner in column 7, lines 49 – 52.

With regard to claim 24, Chen discloses in figure 6 oxidizing after the drain implant has been provided. It is not clear if Chen further teaches comprising the step of providing a rapid thermal anneal after the drain implant has been provided. Gardner further teaches in column 7, lines 49 – 52 comprising a step of providing a rapid thermal anneal after a drain implant has been provided. It would have been further obvious to one of ordinary skill in the art at the time of the present invention to use the rapid thermal annealing step of Gardner in the method of Chen and Gardner in order to activate the drain dopants and remove crystalline damage as taught by Gardner in column 7, lines 49 – 52.

With regard to claim 25, Gardner teaches in column 7, lines 48 – 52 where a rapid thermal anneal comprises heat treating a semiconductor memory in a furnace at a temperature of about 1000 degrees Celsius for about 10 seconds.

Claims 6 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen as applied to claims 1, 3-5, 7, 8, 17 and 19-21 above, and further in view of Miyata (USPAT 5183773).

Chen discloses in figures 3 and 6 – 6f the semiconductor memory device and spacers. It is not clear if Chen teach wherein the semiconductor memory device further includes a periphery including a plurality of logic devices and wherein the spacer-

providing step further includes the step of providing the first spacer and the second spacer concurrently with a plurality of spacers in the periphery of the semiconductor memory device. Miyata teaches in figures 3l – 3m wherein a semiconductor memory device (32) further includes a periphery (34 and 36) including a plurality of logic devices (33 and 35) and wherein a spacer (98) providing step further includes the step of providing a first spacer and a second spacer concurrently with a plurality of spacers in the periphery of the semiconductor memory device. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the peripheral logic devices and concurrent spacer forming step of Miyata in the method of Chen in order to save space on a mother board and therefore reduce costs of fabrication by further consolidating fabrication steps.

Claims 22 – 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen as applied to claim 19 above, and further in view of Shah et al. (USPAT 5065208, Shah).

Chen discloses in column 6, lines 64 – 67 wherein heat treating the semiconductor memory comprises annealing the semiconductor memory at a temperature of 1050 degrees Fahrenheit. Chen does not teach annealing at 900 degrees Celsius for about 40 minutes. Shah teaches in column 10, lines 33 – 37 wherein heat treating a semiconductor memory comprises annealing the semiconductor memory in a furnace at about 900 degrees Celsius for about 40 minutes. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use

the annealing of Shah in the method of Chen in order to drive an N type impurity of a source region under gate oxide as taught by Shah in column 10, lines 33 – 37.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1, 3, 4, 6 – 9, 17 – 19, and 24 – 26 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 – 5 of U.S. Patent No. 6,235,584.

As far as the examiner can ascertain the subject matter of claims 1 and 19 of the application are covered by claim 1 of the patent. The subject matter of claim 3 of the application is covered by claims 1 and 2 of the patent. The subject matter of claim 4 of the application is covered by claim 1 of the patent. The subject matter of claims 6 and 26 of the application are covered by claims 1 and 3 of the patent. The subject matter of claim 7 of the application is covered by claims 1 and 4 of the patent. The subject matter of claim 8 of the application is covered by claims 1 – 5 of the patent. The subject matter

of claims 9, 24, and 25 of the application is covered by claims 1 – 5 of the patent. The subject matter of claims 17 and 18 of the application are covered by claims 1 and 2 of the patent.

Claim 5, 20, 21 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 – 5 of U.S. Patent No. 6,235,584 in view of Chen. It would have been obvious to have the additional features of a self-aligned source etch, DDI implant, and MDDI implant of Chen in the invention of U.S. Patent No. 6,235,584 in order to make a working device.

Claim 22 and 23 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 – 5 of U.S. Patent No. 6,235,584 in view of Shah. It would have been obvious to have the feature of annealing the semiconductor memory in a furnace at about 900 degrees Celsius for about 40 minutes of Shah for the heat treatment in the invention of U.S. Patent No. 6,235,584 in order to drive an N type impurity of a source region under gate oxide.

(10) Response to Argument

- Response regarding claim 1

Appellant argues that Chen does not disclose "providing a drain implant after step (c), the drain implant being provided in the substrate adjacent to the second edge of each of the plurality of gate stacks" as recited in claim 1. This is not persuasive. This

limitation is clearly shown in figures 6 and 6E. Figure 6 shows the process flow of Chen where step 672 (second MDD implant) is performed after step 462 (thermal cycle, which drives the source implant under the first edge of gate stacks as recited in claim 1 step (c)). This clearly shows that Chen discloses performing the drain implant (second MDD implant) as shown in figure 6E after claimed step (c).

In further support of this argument appellant argues that the MDD2 implant (second MDD implant) of Chen is clearly performed simultaneously on the source and drain. Appellant points out that there is no mask applied during the MDD2 implant and that Chen teaches this implant step enhances the doping concentration in the tunneling region, which refers to the tunneling across dielectric 120 between floating gate 122 and source 112. This argument is not persuasive. The term "drain implant" as used in the claims does not necessitate such a narrow interpretation as to necessarily include the use of a mask or preclude the implant step also implanting the source region. The term " drain implant" merely defines a step that implants into the drain region. Using the broadest reasonable interpretation of the term "drain implant", the term cannot be so narrowly construed to define an implantation step into only the drain region. To interpret "drain implant" so narrowly would be improperly reading limitations into the claims.

Appellant further argues that Chen does not use the language of a "drain implant" or the concept of the "drain implant" being performed separately from the source implant as in claim 1. First, Chen does use the term "drain implant" is includes the MDD implant which is taught on column 7 line 2 as being a "medium diffused drain" implant. Thus the language "drain implant" is used by Chen. Note that in the prior art the terms for the

implantations are loosely defined and used. For instance, the implant into only the source region of figure 6C is referred to as a MDD implant even though it clearly is only applied to the source region. This usage of the terminology in the prior art lends further support to the Examiner's broadest reasonable interpretation of the term "drain implant." Further, Chen does have a drain implant performed separately from the source implant. Chen first performs a first (DDI, step 458) and second (MDDI, step 670) source implant, and thereafter performs a "drain implant" (second MDD implant, step 672) that implants dopants into the drain regions. The DDI and MDDI implants are clearly performed separately from the second MDD implant.

Appellant further argues that each mention of the "source implant" and "drain implant" in embodiments of their invention are mutually exclusive and that the source implant is clearly designated as being "only performed for the source." Appellant states that the application clearly teaches a distinctive source implant, and therefore, a distinctive drain implant. This is not persuasive. Even if one were to improperly narrow the claims by reading a specific definition for a term into the claims from the specification, appellants specification nowhere states that the drain implant is limited to **only** being implanting into the drain region. Thus, the specification provides no support for this narrow definition of "drain implant." The fact that appellant's specification does not explicitly mention the interpretation of "drain implant" applied in the rejections does not preclude the reasonably broad interpretation from being used.

To summarize, appellant has argued that Chen does not teach the "drain implant" of their invention since Chen does not perform the drain implant solely in the

drain region. This is not persuasive as explained above since the Examiner is not limited to the improperly narrow interpretation of the claim language that appellant may desire. For these reasons, the Examiner respectfully requests that the rejection of claim 1 be affirmed.

- Response regarding claim 3

Appellant has not presented any further arguments with regard to claim 3. Thus, the Examiner considers the rejection of claim 3 proper for the reasons expressed above with regard to claim 1.

- Response regarding claim 4

Appellant argued that Chen does not disclose the step of "providing a first spacer and a second spacer for each of the plurality of gate stacks, the first spacer being disposed along the first edge of each of the plurality of gate stacks, the second spacer being disposed along the second edge of each of the plurality of gate stacks." This is not persuasive as layer 720 as shown in figure 6F clearly includes a first and second spacer along the first and second edges as claimed.

Appellant argues that insulating layer 720 of Chen is an oxidation sealing layer that is grown over the entire array of gate stacks and thus Chen does not mention spacers along the edge of the gate stacks. This is not persuasive. Insulating layer 720 provides a spacer along each side of the gate stacks since it is formed conformal to the gate stacks (see figure 6F). The fact that layer 720 is an oxidation sealing layer does

not preclude it from also forming the claimed first and second spacer. Also, the fact that layer 720 extends over the top of the gate stacks and over the substrate in the source/drain regions does not change the fact that layer 720 also forms spacers along the sidewalls of the gate stacks. The language of claim 4 merely requires providing a first and second spacer, disposed along the first and second edge of each of the plurality of gate stacks. The language of claim 4 does not require the spacer or the layer the spacer is formed from to not extend over the gate stacks. Thus, though layer 720 of Chen is disposed along structures other than solely the edges of the gate stacks, the layer is still disposed along the edges and therefore constitutes the claimed first and second spacer.

- Response regarding claim 5

Appellant argues that Chen does not disclose the further step of "providing a self-aligned source etch" as recited in claim 5. Appellant argues that element 454 of Chen is performed after masking the drain regions, but before any implant steps have been performed and not as a subsequent step as in claim 5. This is not persuasive. First, it is noted that Chen very clearly teach performing a self-aligned source etch. See element 454 in figure 6 and column 6 lines 46-48 and column 8 lines 28-30 (note that as shown in figure 6, step 454 is part of step 452). Second, it is noted that claim 5 does not require the self-aligned source etch be performed at any particular point during the fabrication sequence. Thus, appellant's argument that element 454 cannot be the claimed "self-aligned source etch" because it is not performed as a subsequent step is

not persuasive. The language of claim 5 does not require the added step be performed at any particular point during the process and thus performing the self-aligned source etch before implantation, as in Chen, anticipates the claimed limitation.

- Response regarding claims 7, 8 and 17

Appellant has not presented any further arguments with regard to these claims. Thus, the Examiner considers the rejection of these claims proper for the reasons expressed above with regard to claim 1.

- Response regarding claim 19

Appellant's arguments regarding claim 19 are essentially the same arguments made regarding claim 1. These arguments have been addressed in detail above. As discussed above, the language of the claims are given no more than their reasonable broadest interpretation. The interpretation given to the term "drain implant" is any implant step that implants into the drain region, regardless of whether the step implants into other regions simultaneously. To narrow the interpretation of the term "drain implant" to only include an implantation step that implants **solely** into the drain region is an improperly narrow interpretation that is not supported by appellant's specification. The second MDD implant of Chen (step 672, figure 6 and 6E) is clearly a "drain implant" as it implants into the drain region and thus Chen properly discloses "performing a drain implant" as recited in claim 19.

- Response regarding claims 20 and 21

Appellant has not presented any further arguments with regard to these claims. Thus, the Examiner considers the rejection of these claims proper for the reasons expressed above with regard to claim 19.

- Response regarding claims 9, 24 and 25

Appellant has argued that the Examiner has not provided a source of motivation for combining Chen with Gardner. This is not persuasive since the rejection of these claims clearly states motivation for combining the references ("in order to activate the drain dopants and remove crystalline damage," Final Office Action P. 5 end of second paragraph) and states the source of the motivation. In this case, the motivation came from Gardner on column 7 lines 49-52.

Appellant further argues that Gardner clearly teaches away from the present invention. Appellant cites portions of Gardner stating that Gardner teaches away from implanting the source region of the substrate. This is not persuasive. Gardner might teach that in their specific application they don't perform a heavily-doped diffusion or implantation into the source region, but Gardner does still implant into the source region. See for example, see region 16 in source side 24, which clearly has had dopants introduced into the region. Further, it is not clear how this teaching is construed as teaching away from the combination. Gardner includes a specific teaching of performing a rapid thermal anneal to remove crystalline damage and activate and drive-in the implanted dopants. Since Chen implants dopants in a similar manner, one

of ordinary skill in the art would clearly be motivated to use the rapid thermal annealing technique of Gardner in the method of Chen.

Appellant further argues that the Examiner's conclusion of obviousness is based on improper hindsight reasoning. Appellant reasoning as to why the Examiner's conclusion is based upon improper hindsight is appellant's belief that Chen does not teach a drain implant. First, it has already been established above with regard to claims 1 and 19 that Chen does teach a drain implant. Second, the rejection using Chen with Gardner has not relied upon any knowledge that was not in Chen and Gardner themselves and thus within the level of ordinary skill at the time of the invention.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Appellant further argues that the combination of Chen with Gardner is not enabling since the method of making a non-volatile flash EEPROM of Chen is not compatible with the process for forming the high performance MOSFET of Gardner. this argument is not persuasive. Chen and Gardner both teach fabrication methods and techniques for forming semiconductor devices including depositing, etching, and doping

semiconducting, conducting, and insulating layers. One of ordinary skill in the art of semiconductor manufacture would recognize that techniques dealing with the formation of layers and structures as well as the manipulation of layers to form structures, can easily be applied from one type of semiconductor device to the next. Though Chen and Gardner specifically form different end structures for different devices, the techniques of the fabrication processes are applicable to both references. For example, they both deal with forming layers on a starting silicon substrate, forming insulators, and forming doped source/drain regions. Thus, even though they may form different devices, they both deal with the same types of fabrication steps. Thus, Gardner's motivation of using a rapid thermal annealing to repair crystalline damage (resulting from implanting into a crystalline region) and activate the dopants (one of ordinary skill in the art would recognize that source/drain dopants are electrically inactive until they are activated) is clearly applicable to Chen's method. thus, the methods of the two references are considered compatible. As to appellants arguments again stating that Gardner teaches away from the combination, Gardner does not explicitly teach that the implantation steps of Chen are detrimental. Thus, a reading of Gardner would not explicitly teach away from implanting the source region in the manner performed by Chen.

- Response regarding claims 6 and 26

Appellant has argued that the Examiner has not provided a source of motivation for combining Chen with Miyata. Appellant argues that Miyata does not teach a drain implant after a source implant has been driven. This is not persuasive since Chen

clearly teaches the claimed drain implant after driving the source implant. Miyata is not relied upon for this teaching. Appellant then argues that Miyata does not disclose a memory device that suffers from short channel effects as pertains to appellant's invention and Miyata does not mention driving a drain or source implant under a gate stack. First, since the claims do not recite a memory device having a short channel or suffering from short channel effects, Miyata lack of the same is irrelevant to the invention as claimed. Second, since the claims do not require driving a drain implant under a gate stack, it is irrelevant as to whether Miyata teach this step or not. Third, since Chen teaches driving the source implant under the gate stack and Miyata was not relied upon for this feature, it is irrelevant to argue that Miyata does not teach this feature. As to appellant arguing against the stated motivation. It is a well known industry goal to integrate as many devices onto a single substrate as possible and to reduce the number of separate fabrication steps. This allows a cost savings per number of devices created and per chip. In using the concurrent spacer formation step of Miyata in the method of Chen, one of ordinary skill in the art would recognize that forming the structures in a single step as opposed to forming them in separate steps, would cut down on the total number of processes performed. Reducing the number of processing steps performed is well known to reduce the fabrication time and costs. Furhter, it has been held that it is well within the skill of the ordinary artisan to perform to steps simultaneously which have previously been performed in sequence is obvious. *In re Tatincloux* 108 USPQ 125 (CCPA 1955).

Appellant also argues that the Examiner is using improper hindsight reasoning in combining Chen with Miyata. This argument is not persuasive. It is well known in the art of semiconductor manufacturing that a consolidation of process steps is advantageous. Each separate step that can be eliminated in the fabrication of semiconductor devices results in being able to make the devices quicker and cheaper.

- Response regarding claims 22 and 23

Appellant argues that the Examiner has not presented a source for the motivation to modify Chen with Shah. This is not persuasive. As stated in the final rejection, page 7 end of second paragraph, the motivation for using the annealing step of Shah is given in Shah column 10 lines 33-37.

Appellant further argues that the Examiner used improper hindsight reasoning in combining Chen with Shah. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). In the instant case, the teachings and motivation come from the references themselves and thus the rejection takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made. Appellant furthers

this argument by stating that Shah does not teach annealing a semiconductor memory. This is not persuasive. Shah teaches a heating treatment that is specifically used to drive an n-type impurity of a source region under a gate oxide. This is the same step that Chen performs with their heat treatment step. However, Chen is silent as to all of the process conditions during their heat treatment step. Thus, one would look towards Shah for the process conditions since Shah teaches the same heat treatment step for the same result. Thus, one would still be motivated to use the heat treatment step of Shah in the method of Chen regardless of the minor differences in the teachings of the references.

Appellant further argues that the process of Chen is not compatible with the process of Shah and thus the combination is not enabling. This is not persuasive since both processes deal with the deposition, patterning, etching, implanting and annealing of layers on a semiconductor substrate. Both references are concerned with annealing after a source implantation to drive the n-type impurity under the gate oxide. Thus, these references are clearly compatible. The fact that Shah teaches annealing both the source and drain simultaneously does not change the fact that Shah teaches process conditions that will allow a semiconductor structure to be annealed in a manner to diffuse the source implant under the edge of the gate such as in Chen. The process conditions of Shah are clearly applicable to Chen and thus would not create an inoperable reference when combined. Thus, the combination is enabling.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

N. Drew Richards

AU 2815

Conferees:

Ken Parker

Darren Schuberg

SPE Kenneth Parker
TC2800